ABSTRACT OF THE DISCLOSURE

0026 Hard mask trimming with a thin hard mask layer and a top protection layer is disclosed. During fabrication of a semiconductor device, the device has a primary layer, a lower layer, and an upper layer. The primary layer, which may be a polysilicon layer, has a critical dimension specification. The lower layer is over the polysilicon layer, and is subsequently hard mask trimmed to satisfy the critical dimension specification of the primary layer. The upper layer is over the lower layer, and has a high-etching selectivity as compared to the lower layer. The upper layer substantially prevents thickness loss of the lower layer during hard mask trimming. Each of the upper layer and the lower layer may be Si_3N_4, SiON, or SiO_2. Additionally, the upper layer may be polysilicon.